Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (original) A method comprising:

fetching data from a cache in a computer;

during the fetching, detecting a soft error in the data;

as a result of detecting the soft error, stalling the computer;

performing a clearing operation to clear the soft error; and

resuming fetching of the data.

2. (original) The method of claim 1, wherein the clearing operation comprises clearing the entire cache.

3. (original) The method of claim 1, wherein the clearing operation comprises clearing the cache line containing the soft error.

4. (original) The method of claim 1, wherein the clearing operation comprises clearing an intermediate portion of the cache containing the soft error.

5. (original) The method of claim 1, wherein the error is detected by comparing an expected parity of the cache line with a calculated parity of the cache line.

6. (original) A system comprising:

a memory;

a processor coupled to the memory;

a cache coupled to the processor;

soft error detection logic coupled to the cache to detect soft errors therein;

soft error handling decision logic coupled to the soft error detection logic to perform one of a plurality of operations based on an input from the soft error detection logic; and

a soft error handler invokable by the soft error handling decision logic to perform one of operations to clear the soft error.

7. (original) The system of claim 6, wherein the operations to clear the soft error include one of flushing the cache, invalidating a cache line, or clearing an intermediate portion of the cache.

8. (original) The system of claim 6, further comprising a soft error recovery memory to store information associated with recovering from a soft error.

9. (original) The system of claim 8, wherein the information is an address of a cache line containing a soft error.

10. (original) The system of claim 8, wherein the soft error recovery memory comprises a register.

11. (currently amended) The system of claim 6, wherein the soft error detection logic is ~~configured~~ to compare an expected parity of a cache line with a calculated parity of the cache line.

12. (currently amended) The system of claim 6, wherein the soft error handling decision logic comprises a multiplexer ~~configured~~ to select as input one of data corresponding to a cache line currently being fetched and a request to invoke the soft error handler, depending on a value of an output of the soft error detection logic.

13. (currently amended) A system comprising:

a cache;

soft error detection logic coupled to the cache; and

decision logic ~~having~~ to receive at least first, second and third ~~inputs~~ input values, the first input value being a request to invoke a soft error handler, the second input value corresponding to data in a cache line of the instruction cache ~~;~~ , and the third input value being an indicator from the soft error detection logic to indicate whether a soft error is present in the data in the cache line.

14. (currently amended) The system of claim 13, further comprising a register ~~configured~~ to store an address of a cache line containing data currently being fetched.

15. (currently amended) The system of claim 13, wherein the soft error detection logic is ~~configured~~ to compare an expected parity of the data, and a calculated parity of the data.

16. (original) The system of claim 13, further comprising a soft error handler invokable by the request.

17. (original) A method comprising:

executing at least a portion of a sequence of computer instructions, at least one of the instructions being stored in a cache;

before fetching the at least one instruction from the cache for execution, determining whether the cache line contains a soft error; and

if it is determined that the cache line contains a soft error,

storing the address of the cache line corresponding to the at least one instruction in a register; and

issuing a request to a soft error handler to clear the soft error.

18. (original) The method of claim 17, wherein the soft error handler:

stops fetching of instructions from the cache;

reads the address in the register; and

clears the corresponding cache line.

19. (original) The method of claim 17, further comprising resuming execution of the sequence of computer instructions at the instruction corresponding to the cleared cache line.

20. (original) A computer-usable medium storing computer-executable instructions which, when executed by a processor, implement a process comprising:

in response to a request resulting from detection of a soft error in data in a cache line of a cache,

stopping fetching of data from the cache without shutting down;

performing one of clearing the cache, clearing the cache line containing the soft error, and clearing an intermediate portion of the cache containing the soft error; and

resuming fetching of data from the cache.

21. (original) The computer-usable medium of claim 20, the process further including reading a memory storing an address of the cache line.

22. (original) The computer-usable medium of claim 20, the process further including invalidating the cache line.